MMIC DESIGNERS TRAINED ON REAL CHIPS WITHOUT EXPENSIVE FABRICATION

James C. M. Hwang

Lehigh University, 5 East Packer Avenue, Bethlehem PA 18015 USA

ABSTRACT—**Without many lengthy and expensive design/fabrication/test iterations, we have trained a number of MMIC designers who can contribute to the industry even before they graduate. The approach involves mainly large-signal modeling and internal-node microwave waveform probing of existing MMIC chips. Typically, it starts by a company asking us to help diagnose a certain MMIC. Students then extract large-signal transistor models themselves and use the models to simulate the internal-node waveforms of the MMIC. By comparing the modeled and measured results, students gain insight of the MMIC working principles. Next, design improvement is suggested and verified by novel cutting and pasting techniques. Lastly, by focusing on microwave waveforms students are proficient in both frequency- and time-domain techniques, making them particularly suitable for modern wireless communication applications which involve complex signal-modulation schemes.**

I. Introduction

One of the most important MMIC applications involves RF/microwave power amplifiers. However, in spite of the advance in nonlinear large-signal modeling and analysis, most MMIC power amplifiers have been designed based on small-signal models and empirical load-pull data. Using such an approach, many design/fabrication/test iterations are often required to meet the performance specifications. With conflicting goals such as (1) higher performance for increasingly complicated signal-modulation schemes, (2) time-to-market even more important than superior performance, and (3) cost being the king, it is obvious that nonlinear large-signal modeling and analysis should be used to design the amplifiers from the beginning or, at least, to guide design modification between iterations.

Since old habits are difficult to break, we set out to train a new breed of MMIC designers who have hands-on experience with nonlinear large-signal modeling and analysis thereby are convinced of their utility. Upon entering the industry, these new designers can quickly impact the company bottom line by using large-signal models to make the current empirical practice more efficient, before attempting to start a revolution by insisting on doing everything right from scratch.

Notice that nowadays few companies and universities can afford the design/fabrication/test cycles solely for training purposes. Shared MMIC fabrication similar to the MOSES program for digital IC's has been impractical because present MMIC designers require extensive engineering support form the wafer foundry. For the same reason, MMIC designers trained in virtual environment tend to have unrealistic expectations.

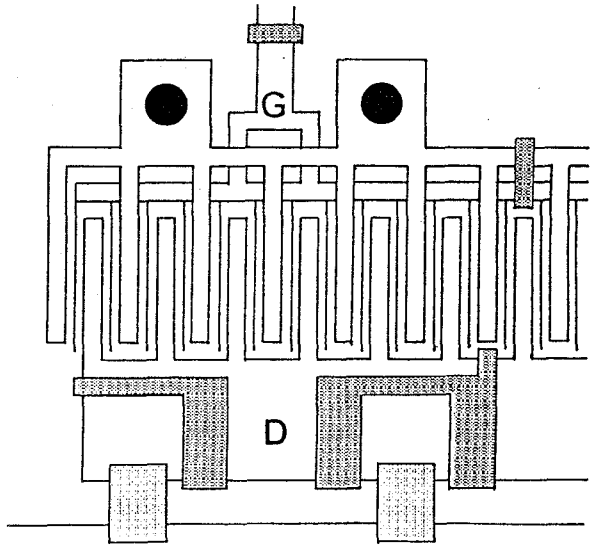

Fig. 1 A transistor cell cut from the output stage of a multistage MESFET MMIC amplifier. (•) through-substrate via. (▨) area cut by focused ion beam. (▩) paste-on metal along the chip edge. **(G)** MESFET gate. **(D)** MESFET drain.

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II. Approaches

As usual, large-signal circuit analysis starts from large-signal transistor modeling. Since most companies either have large-signal transistor models of doubtful validity or no large-signal model at all, it is necessary to extract the models ourselves. Ideally, models can be extracted from discrete devices of various sizes that are fabricated together on the MMIC wafer as process-control monitors. If suitable discrete devices are not available it will be necessary to cut them out of an MMIC and paste ground pads on the input/output lines to facilitate microwave probing.

Fig. 1 illustrates how cells of different sizes are cut from the output stage of a MESFET multistage power amplifier. Usually cutting is done by focused ion-beam etching, laser ablation, or ultrasonic probing, depending on the trade off between precision and cost. In the case shown in Fig. 1, because the output matching network is placed off chip (for improved power-added efficiency), the output ground pads can be pasted along the edge of the chip using a probe which has been dipped in silver epoxy. Alternatively selective metal deposition can be done by a focused ion beam albeit very slowly. design. Input grounding has already been provided by the through-substrate vias which are integral to the MMIC design.

In other cases a small chip [1] containing suitable prob contact pads and a transmission line stub is mounted abut the MMIC chip. The transmission line stub is then connected via a short bond wire to a suitable location along the input or output line of the transistor (Fig. 2). Using similar cutting and pasting techniques, an MMIC can be dissected while splicing on passive elements or diodes to test circuit design modification hypotheses.

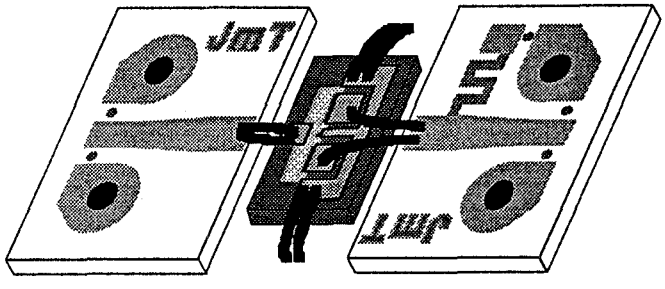

Fig. 2 An internal cell connected via short bond wires to adjacent chips which contain suitable probe contact pads. (•) through-substrate via.

From properly configured transistors, large-signal models are extracted and verified (including scaling) from dc characteristics and microwave scattering parameters in the conventional manner. The models are constructed in popular commercial simulation tools [2] utilizing user-defined elements. Additional fine-tuning and model verification are performed through comparison with input/output current and voltage waveforms [3] that are measured by the technique described below. By combining large-signal transistor models with passive element models based on the MMIC layout, internal-node waveforms as well as MMIC input/output characteristics are simulated using the same commercial simulation tool.

Fig. 3 shows that the internal waveform probing setup involves mainly a high-impedance microwave probe and a microwave transition analyzer [4]. The contacting probe facilitate accurate calibration at both dc and RF levels. The high impedance of the probe presents little perturbance to the MMIC under test in real operating conditions. This is especially true for power amplifiers which tend to have relatively low internal impedances. The probe has a single tip (without any grounding contact) hence can be used anywhere on the MMIC without special test patterns. This is in contrast to the above described transistor probing for model extraction purpose in which ground pads must be provided to maintain a 50 Ω environment all the way to the probe tip.

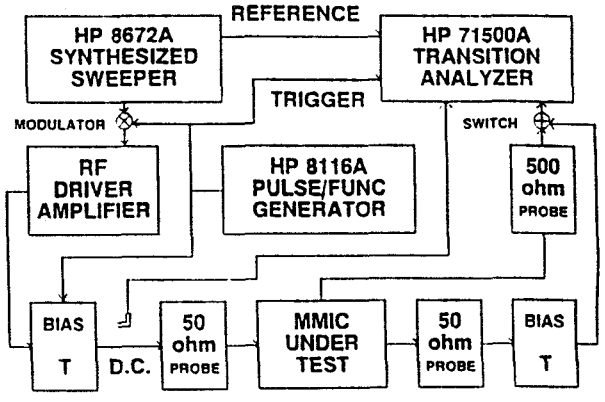

Fig. 3 Pulsed internal-node microwave waveform measurement setup.

The transition analyzer uses a harmonic sampling technique to obtain both frequency- and time-domain information. In particular, both the magnitudes and phases of the harmonic components of a microwave signal are measured which can then be used to reconstruct the voltage waveform in time domain.

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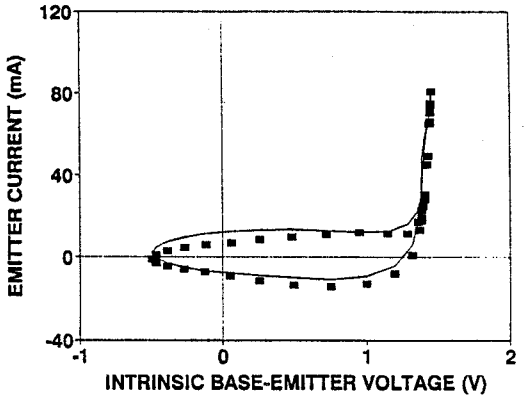
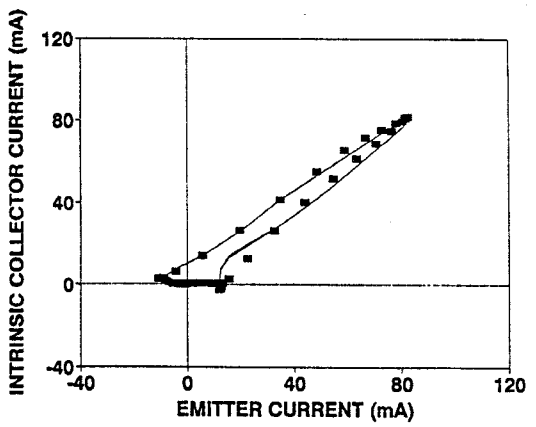
Using standard frequency-domain techniques, the measurement set up is readily calibrated and the measured harmonics rotated to an internal node of the MMIC. From voltage waveforms measured on two internal nodes separated by a known impedance, current waveform is calculated. From the ratio of voltage and current waveforms, internal load impedances are determined at each harmonic frequency. Recently, the above described technique was modified to allow pulsed internal waveform probing of MMIC's that are designed either for pulsed operation or flip-chip packaging [5]. This shows that the present technique can work equally well on MMIC's of either microstrip or coplanar design.



(a)

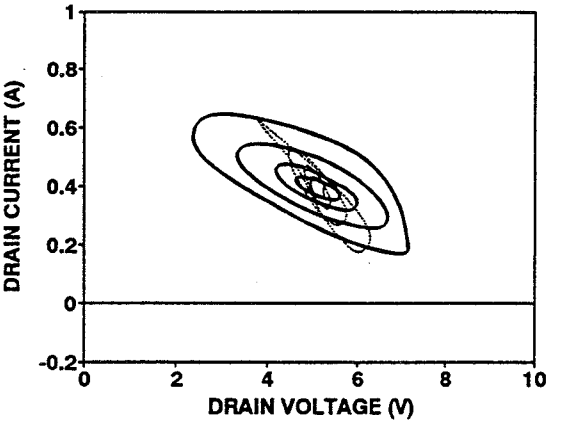


(b)

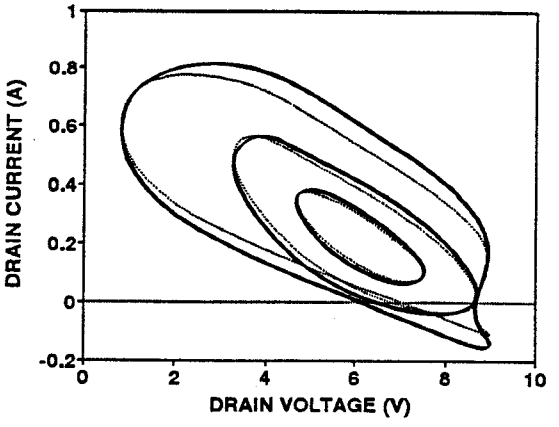
Fig. 4 (—) Modeled vs. (■) measured intrinsic (a) emitter and (b) collector characteristics of an HBT under Class C operation. V_{BE} = 0.8 V. V_{CE} = 4 V. P_{IN} = 11 dBm @ 2 GHz.

III. Results and Discussion

Using the above approaches, we have helped a number of companies such as Anadigics, Hughes, ITT, Raytheon, Rockwell and TI to diagnose and improve their MESFET, HFET and HBT MMIC power amplifiers while educating our students. A few examples are illustrated in the following.



(a)



(b)

Fig. 5 Dynamic load lines of second-stage (—) inner and (- - -) outer cells measured on a MESFET coplanar power amplifier (a) before and (b) after design modification. The dynamic load lines are measured at 5 μs after pulsing V_{GG} from = 0.-6 to -1.6 V for 10 μs with a repetition rate of 200 Hz. V_{DD} = 7 V. P_{IN} = 5, 11, 17 and 23 dBm in (a) and 5, 11 and 17 dBm in (b). f = 2 GHz.

Fig. 4 shows the results of a large-signal transistor model extracted from a GaAs/AlGaAs HBT having an emitter area of approximately 300 μm^2 [3]. The model was extracted with the help of large-signal waveforms which allowed the collector transit time to be separated from the total delay. This is particularly important for power HBT's which tend to have a thick collector and its structure must be optimized for high breakdown voltage with adequate current capacity and switching speed. It can be seen that the modeled and measured intrinsic emitter and collector characteristics are in reasonable agreement.

Fig. 5 compares the measured dynamic load lines of a two-stage GaAs MESFET coplanar MMIC power amplifier before and after design modification [7]. The second stage of the amplifier comprises four transistor cells which are arrayed in a direction perpendicular to the line of symmetry which connects the MMIC input with its output. The two cells that are closer to the line of symmetry are designated as inner cells while the remaining two cells that are closer to the edges of the MMIC are designated as outer cells. As seen in Fig. 5a, before modification, the outer cells are improperly load-matched thereby contribute little output power. By interaction through the power combining lines, the inner cells are also mismatched although not as severely. After modification, the inner and outer cells both are matched and have adequate output powers.

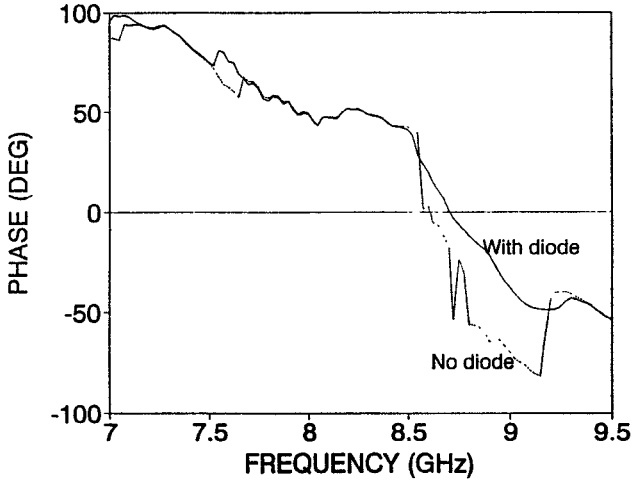


Fig. 6 Insertion phases of a three-stage HFET power amplifier measured (—) with and (...) without bias-stabilization diodes. V_{GG} = - 1.2 V. V_{DD} = 6 V. P_{IN} = 2 dBm.

Fig. 6 shows that a three-stage GaAs/AlGaAs HFET power amplifier exhibits sudden phase changes within the bandwidth of 7 to 9.5 GHz [8]. By probing the input and output of each of the three stages, it was found that the phase discontinuity originated mainly from the third stage where it was driven into heavy compression. In-depth simulation and analysis led to the conclusion that the phase discontinuity was due to a complicated interaction between premature breakdown and self biasing. An approach to reduce the phase discontinuity by clamping down the gate bias voltage with diodes was therefore hypothesized and verified experimentally as shown in the figure.

IV. Conclusion

Approaches to train MMIC designers with hands-on experience of large-signal modeling and analysis were developed using internal-node microwave waveform probing of existing MMIC chips in conjunction with novel cutting and pasting techniques. By comparing the modeled and measured results, students gain insight of the MMIC working principles while helping companies solve real problems. Thus, upon entering the industry, these students can hit the ground and run, while gradually tranform the current practice of MMIC designers.

Acknowledgment

The author is indebted to the assistance of the coauthors listed under [3] to [8].

References

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